UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,312	09/22/2003	Joseph John Sumakeris	5000.319	2311

21176 7590 03/11/2005

SUMMA & ALLAN, P.A.
11610 NORTH COMMUNITY HOUSE ROAD
SUITE 200
CHARLOTTE, NC 28277

EXAMINER	
CHEN, ERIC BRICE	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 03/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,312	SUMAKERIS, JOSEPH JOHN	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 9/22/03.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-30 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 9/22/03 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5/3/04.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

CB

DETAILED ACTION

Priority

1. Applicant is advised of possible benefits under 35 U.S.C. 119(a)-(d), wherein an application for patent filed in the United States may be entitled to the benefit of the filing date of a prior application filed in a foreign country.

Drawings

2. The drawings are objected to because Figure 2 lacks a reference character "14". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 2 is objected to because of the following informalities: "first isotropic etch" should apparently be -- first non-selective etch --. Claim 1 does not contain any language referring to a "first isotropic etch." Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 7-15, and 17-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Powell (U.S. Patent No. 5,915,194), in view of Nishiguchi et al., *Journal of Crystal Growth*, vol. 237-239 (2002) and Inoguchi (U.S. Patent No. 5,900,647).

6. As to claim 1, Powell discloses a method of preparing a substrate for reducing stacking fault nucleation and reducing forward voltage (V_f) drift in silicon carbide-based bipolar devices, the method comprising: conducting a first non-selective etch on the surface of a silicon carbide substrate (24) (column 11, lines

14-20) to remove both surface and subsurface damage (column 11, lines 49-53); and growing a conductive epitaxial layer on the etched substrate surface (column 12, lines 44-56). Powell does not expressly disclose the steps of: conducting a selective etch on the same surface sufficient to delineate the basal plane dislocations with the wafer surface and that will thereafter tend to terminate or to propagate as threading defects while avoiding creating beta (3C) inclusions and carrot defects; growing a conductive epitaxial layer on the selectively etched substrate surface to a thickness greater than that of the typical threading dislocation etch pit depth in the selectively-etched surface to thereby provide the epitaxial layer with a sufficient thickness to support additional polishing and etching steps above the substrate; polishing away a sufficient portion of the conductive epitaxial layer to remove the material containing the etched pits to thereby provide a surface with fewer etched pits than the surface of the selectively-etched substrate; and conducting a second non-selective etch of the epilayer sufficient to remove subsurface damage from the step of polishing the epitaxial layer but without reaching the underlying substrate, to thereby reduce the number of sub-surface defects that can propagate stacking faults under forward voltage in a device formed on the substrate and the polished epilayer.

7. Powell teaches that in order to deposit low-defect SiC crystal films (column 7, lines 66-67), the step-flow growth mechanism is favored over the two-dimensional nucleation (column 8, lines 7-13). Steps are generated by slicing the SiC wafer such that there is a small tilt angle relative to the (0001) basal plane (column 8, lines 9-11), preferably with a tilt angle less than 8° (column 4,

lines 48-51). Powell further teaches that a tilt angle towards a <1120> direction (Figure 2) produces optimum growth rates and crystal quality (column 11, lines 17-20). Nishiguchi teaches that etching SiC with molten KOH (page 1240, column 1) produces hexagonal etch pits towards <1120> directions (page 1240, column 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of: conducting a selective etch on the same surface sufficient to delineate the basal plane dislocations with the wafer surface and that will thereafter tend to terminate or to propagate as threading defects while avoiding creating beta (3C) inclusions and carrot defects. One who is skilled in the art would be motivated to include a KOH etch to produce hexagonal etch pits towards <1120> directions and to produce an off-axis tilt to favor step-flow growth, producing high-quality SiC crystals.

8. Inoguchi discloses the deposition of an epitaxial SiC layer (2) on SiC substrate (1) (column 5, lines 20-24). Inoguchi teaches that any polishing damage incurred during the preparation of substrate (1) results in a greater number of defects in SiC layer (2) (column 7, lines 19-27). Inoguchi further teaches that the growth of the SiC layer (2) to about twenty times greater than the damaged surface portion reduces the number of defects in the epitaxial SiC film (column 7, lines 19-27; column 5, lines 2-6). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of: growing a conductive epitaxial layer on the selectively etched substrate surface to a thickness greater than that of the typical threading dislocation etch pit depth in the selectively-etched surface to thereby provide the

epitaxial layer with a sufficient thickness to support additional polishing and etching steps above the substrate. One who is skilled in the art would be motivated to deposit the epitaxial SiC film at a greater thickness to reduce the number of defects.

9. Powell teaches that presence of defects within the SiC crystal, including micropipes and dislocations, adversely affects the electrical properties of any semiconductor device formed with the SiC crystal (column 3, lines 65-67; column 4, lines 1-5). Powell further teaches that once a SiC surface has been polished, it is subjected to various pregrowth treatments, including oxidation, chemical mechanical polishing, or reactive ion etching (column 11, lines 49-53). Steps to remove contamination and defects on the surface of the substrate are necessary, because defects act as unwanted sites for two-dimensional nucleation of the SiC epitaxial film (column 11, lines 55-59). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the steps of: polishing away a sufficient portion of the conductive epitaxial layer to remove the material containing the etched pits to thereby provide a surface with fewer etched pits than the surface of the selectively-etched substrate; and conducting a second non-selective etch of the epilayer sufficient to remove subsurface damage from the step of polishing the epitaxial layer but without reaching the underlying substrate, to thereby reduce the number of sub-surface defects that can propagate stacking faults under forward voltage in a device formed on the substrate and the polished epilayer. One who is skilled in the art would be motivated to reduce the number of defect in the SiC film.

10. As to claim 2, Powell discloses that the step of conducting the first isotropic etch comprises conducting a reactive ion etch (column 11, lines 49-53).

11. As to claim 3, Nishiguchi discloses conducting the selective etch comprises etching the surface with a molten salt (page 1240, column 1).

12. As to claim 4, Nishiguchi discloses etching the surface with molten potassium hydroxide (page 1240, column 1).

13. As to claim 7, Powell discloses the steps of sawing a silicon carbide substrate wafer from a silicon carbide boule (column 11, lines 14-15); and thereafter conducting the nonselective etch on the substrate wafer (column 11, lines 49-53).

14. As to claim 8, Powell discloses lapping and polishing (column 11, lines 20-22) the sawed substrate wafer and prior to conducting the nonselective etch (column 11, lines 49-53).

15. As to claim 9, Powell does not expressly disclose growing the first device epitaxial layer immediately on the surface prepared by the second non-selective etch. However, Powell's method is directed at producing atomically-flat, low-defect single crystal surfaces (column 7, lines 35-37) to produce a large variety of semiconductor devices (column 3, lines 4-17). Powell further teaches that additional growth procedures can produce multi-layered doped SiC structures (column 7, lines 54-56). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of: growing the first device epitaxial layer immediately on the surface prepared by the second non-selective etch. One who is skilled in the art would be motivated

to form the SiC device on a substrate containing a low number of crystalline defects.

16. As to claim 10, Powell discloses conducting the non-selective and selective etches on a single crystal substrate having a polytype selected from the 3C, 4H, 6H and 15R polytypes of silicon carbide (column 8, lines 39-40).

17. As to claim 11, Powell discloses a method of preparing a substrate and epilayer for reducing stacking fault nucleation and reducing forward voltage (V_f) drift in silicon carbide-based bipolar devices, the method comprising: etching the surface of a silicon carbide substrate with a nonselective etch to remove both surface and subsurface damage (column 11, lines 49-53); and thereafter growing a first epitaxial layer of silicon carbide on the etched surface (column 12, lines 44-56). Powell does not expressly disclose etching the same surface with a selective etch to thereby develop etch-generated structures from at least any basal plane dislocations structures on the substrate that will thereafter tend to either terminate or to propagate as threading dislocations during subsequent epilayer growth on the substrate surface.

18. Powell teaches that in order to deposit low-defect SiC crystal films (column 7, lines 66-67), the step-flow growth mechanism is favored over the two-dimensional nucleation (column 8, lines 7-13). Steps are generated by slicing the SiC wafer such that there is a small tilt angle relative to the (0001) basal plane (column 8, lines 9-11), preferably with a tilt angle less than 8° (column 4, lines 48-51). Powell further teaches that a tilt angle towards a <1120> direction (Figure 2) produces optimum growth rates and crystal quality (column 11, lines

17-20). Nishiguchi teaches that etching SiC with molten KOH (page 1240, column 1) produces hexagonal etch pits towards <1120> directions (page 1240, column 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of: etching the same surface with a selective etch to thereby develop etch-generated structures from at least any basal plane dislocations structures on the substrate that will thereafter tend to either terminate or to propagate as threading dislocations during subsequent epilayer growth on the substrate surface. One who is skilled in the art would be motivated to include a KOH etch to produce hexagonal etch pits towards <1120> directions and to produce an off-axis tilt to favor step-flow growth, producing high-quality SiC crystals.

19. As to claim 12, Powell discloses etching the surface with a reactive ion etch as the nonselective etch (column 11, lines 49-53).

20. As to claim 13, Powell discloses etching the surface with a chemical mechanical polishing step (column 11, lines 49-53).

21. As to claim 14, Nishiguchi discloses conducting the selective etch comprises etching the surface with a molten salt (page 1240, column 1).

22. As to claim 15, Powell discloses growing a conductive epitaxial layer on the twice-etched surface (column 12, lines 44-56).

23. As to claim 18, Powell does not expressly disclose that the step of growing the first epitaxial layer comprises forming a semi-sacrificial epitaxial layer on the selectively etched surface to encourage the etched basal plane defects to reorient during subsequent growth into threaded defects; and further comprising

the steps of: polishing the etched semi-sacrificial epitaxial layer to reduce etch pits; and etching the polished semi-sacrificial epitaxial layer to remove subsurface damage from the step of polishing the epitaxial layer but without reaching the underlying substrate, to thereby reduce the number of subsurface defects that can propagate stacking faults under forward voltage in a device formed on the substrate and the polished epilayer; all prior to forming the first epitaxial layer.

24. Inoguchi discloses the deposition of an epitaxial SiC layer (2) on SiC substrate (1) (column 5, lines 20-24). Inoguchi teaches that any polishing damage incurred during the preparation of substrate (1) results in a greater number of defects in SiC layer (2) (column 7, lines 19-27). Inoguchi further teaches that the growth of the SiC layer (2) to about twenty times greater than the damaged surface portion reduces the number of defects in the epitaxial SiC film (column 7, lines 19-27; column 5, lines 2-6). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of: forming a semi-sacrificial epitaxial layer on the selectively etched surface to encourage the etched basal plane defects to reorient during subsequent growth into threaded defects. One who is skilled in the art would be motivated to deposit the epitaxial SiC film at a greater thickness to reduce the number of defects.

25. Powell teaches that presence of defects within the SiC crystal, including micropipes and dislocations, adversely affects the electrical properties of any semiconductor device formed with the SiC crystal (column 3, lines 65-67; column

4, lines 1-5). Powell further teaches that once a SiC surface has been polished, it is subjected to various pregrowth treatments, including oxidation, chemical mechanical polishing, or reactive ion etching (column 11, lines 49-53). Steps to remove contamination and defects on the surface of the substrate are necessary, because defects act as unwanted sites for two-dimensional nucleation of the SiC epitaxial film (column 11, lines 55-59). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the steps of: polishing the etched semi-sacrificial epitaxial layer to reduce etch pits; and etching the polished semi-sacrificial epitaxial layer to remove subsurface damage from the step of polishing the epitaxial layer but without reaching the underlying substrate, to thereby reduce the number of subsurface defects that can propagate stacking faults under forward voltage in a device formed on the substrate and the polished epilayer; all prior to forming the first epitaxial layer. One who is skilled in the art would be motivated to deposit the epitaxial SiC film at a greater thickness to reduce the number of defects.

26. As to claim 19, Inoguchi discloses forming the semi-sacrificial epitaxial layer by chemical vapor deposition (column 5, lines 36-37).

27. As to claims 20-22, Inoguchi does not expressly disclose polishing the etched semi-sacrificial epitaxial layer using a chemical-mechanical process, a dry etch, or a reactive ion etch. Powell teaches that presence of defects within the SiC crystal, including micropipes and dislocations, adversely affects the electrical properties of any semiconductor device formed with the SiC crystal (column 3, lines 65-67; column 4, lines 1-5). Powell further teaches that once a SiC surface

has been polished, it is subjected to various pregrowth treatments, including oxidation, chemical mechanical polishing, or reactive ion etching (column 11, lines 49-53). Steps to remove contamination and defects on the surface of the substrate are necessary, because defects act as unwanted sites for two-dimensional nucleation of the SiC epitaxial film (column 11, lines 55-59). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of: polishing the etched semi-sacrificial epitaxial layer using a chemical-mechanical process. One who is skilled in the art would be motivated to reduce the number of defect in the SiC film.

28. As to claim 23, Powell discloses the steps of: sawing the substrate from a single crystal boule (column 11, lines 14-15); lapping the sawed substrate (column 11, lines 20-22); polishing the lapped substrate (column 11, lines 20-22); and cleaning the polished substrate; all prior to the nonselective etch.

29. As to claim 24, Powell discloses a method of preparing and a substrate and epilayer for reducing stacking fault nucleation and reducing forward voltage (V_f) drift in silicon carbide-based bipolar devices, the method comprising: etching the surface of a silicon carbide substrate from which surface and subsurface damage have been removed (column 11, lines 49-53); and thereafter growing a first conductive epitaxial layer of silicon carbide on the etched surface (column 12, lines 44-56). Powell does not expressly disclose: etching the surface of a silicon carbide substrate from which surface and subsurface damage have been removed with a selective etch to thereby develop etch-generated structures from

at least any basal plane dislocations on the substrate that will thereafter tend to either terminate or to propagate as threading dislocations during subsequent epilayer growth on the substrate surface.

30. Powell teaches that in order to deposit low-defect SiC crystal films (column 7, lines 66-67), the step-flow growth mechanism is favored over the two-dimensional nucleation (column 8, lines 7-13). Steps are generated by slicing the SiC wafer such that there is a small tilt angle relative to the (0001) basal plane (column 8, lines 9-11), preferably with a tilt angle less than 8° (column 4, lines 48-51). Powell further teaches that a tilt angle towards a <1120> direction (Figure 2) produces optimum growth rates and crystal quality (column 11, lines 17-20). Nishiguchi teaches that etching SiC with molten KOH (page 1240, column 1) produces hexagonal etch pits towards <1120> directions (page 1240, column 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of: etching the surface of a silicon carbide substrate from which surface and subsurface damage have been removed with a selective etch to thereby develop etch-generated structures from at least any basal plane dislocations on the substrate that will thereafter tend to either terminate or to propagate as threading dislocations during subsequent epilayer growth on the substrate surface. One who is skilled in the art would be motivated to include a KOH etch to produce hexagonal etch pits towards <1120> directions and to produce an off-axis tilt to favor step-flow growth, producing high-quality SiC crystals.

31. As to claim 25, Powell discloses etching the surface of the silicon carbide substrate with a nonselective etch to remove both surface and subsurface damage (column 11, lines 49-53) prior to the step of etching the surface with the selective etch.

32. As to claim 26, Powell discloses the steps of: sawing the substrate from a single crystal boule (column 11, lines 14-15); lapping the sawed substrate (column 11, lines 20-22); polishing the lapped substrate (column 11, lines 20-22); and cleaning the polished substrate (column 11, lines 49-53); all prior to the nonselective etch.

33. As to claim 27, Powell discloses etching the surface with a reactive ion etch as the nonselective etch (column 11, lines 49-53).

34. As to claim 28, Powell discloses etching the surface with a chemical mechanical polishing step (column 11, lines 49-53).

35. As to claim 29, Nishiguchi discloses conducting the selective etch comprises etching the surface with a molten salt (page 1240, column 1).

36. Claims 5-6, 16-17, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Powell, in view of Nishiguchi and Inoguchi, in further view of Streetman, *Solid State Electronic Devices*, 3rd ed., Prentice Hall (1990).

37. As to claim 5, Powell does not expressly disclose forming a bipolar device by: forming a n-type epitaxial layer above the polished and etched surface of the epitaxial layer; and forming a p-type epitaxial layer above the polished and etched surface of the epitaxial layer, with a p-n junction between the n-type and p-type epitaxial layers. However, Powell's method is directed at producing

atomically-flat, low-defect single crystal surfaces (column 7, lines 35-37) to produce a large variety of semiconductor devices (column 3, lines 4-17). Powell further teaches that additional growth procedures can produce multi-layered doped SiC structures (column 7, lines 54-56). Streetman further teaches most semiconductor devices contain at least one p-n junction, which is fundamental to the performance of functions such as rectification, amplification, switching, and other functions (page 130). Streetmen further teaches that epitaxially grown junctions are widely used to form a sharp, single crystal junction by changing doping during crystal growth (page 131). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the steps of: forming a n-type epitaxial layer above the polished and etched surface of the epitaxial layer; and forming a p-type epitaxial layer above the polished and etched surface of the epitaxial layer, with a p-n junction between the n-type and p-type epitaxial layers. One who is skilled in the art would be motivated to form a p-n junction, a structure fundamental to the performance of many semiconductor functions, on the SiC substrate.

38. As to claim 6, Inoguchi discloses: etching an n-type silicon carbide substrate (column 5, lines 29-41); and growing, an n epitaxial layer on the selectively etched substrate surface (column 5, lines 20-24). Inoguchi does not expressly disclose: growing, polishing and etching an n epitaxial layer on the selectively etched substrate surface; growing another n-type epitaxial layer above the polished and etched epitaxial layer; and growing a p-type epitaxial

layer above the n-type epitaxial layer, with a p-n junction between the n-type and p-type epitaxial layers.

39. Powell teaches that presence of defects within the SiC crystal, including micropipes and dislocations, adversely affects the electrical properties of any semiconductor device formed with the SiC crystal (column 3, lines 65-67; column 4, lines 1-5). Powell further teaches that once a SiC surface has been polished, it is subjected to various pregrowth treatments, including oxidation, chemical mechanical polishing, or reactive ion etching (column 11, lines 49-53). Steps to remove contamination and defects on the surface of the substrate are necessary, because defects act as unwanted sites for two-dimensional nucleation of the SiC epitaxial film (column 11, lines 55-59). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the steps of: growing, polishing and etching an n epitaxial layer on the selectively etched substrate surface. One who is skilled in the art would be motivated to reduce the number of defect in the SiC film.

40. Inoguchi teaches that any polishing damage incurred during the preparation of substrate (1) results in a greater number of defects in SiC layer (2) (column 7, lines 19-27). Inoguchi further teaches that the growth of the SiC layer (2) to about twenty times greater than the damaged surface portion reduces the number of defects in the epitaxial SiC film (column 7, lines 19-27; column 5, lines 2-6). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of: growing another n-type epitaxial layer above the polished and etched epitaxial layer. One who is skilled

in the art would be motivated to deposit the epitaxial SiC film at a greater thickness to reduce the number of defects.

41. Powell's method is directed at producing atomically-flat, low-defect single crystal surfaces (column 7, lines 35-37) to produce a large variety of semiconductor devices (column 3, lines 4-17). Powell further teaches that additional growth procedures can produce multi-layered doped SiC structures (column 7, lines 54-56). Streetman further teaches most semiconductor devices contain at least one p-n junction, which is fundamental to the performance of functions such as rectification, amplification, switching, and other functions (page 130). Streetmen further teaches that epitaxially grown junctions are widely used to form a sharp, single crystal junction by changing doping during crystal growth (page 131). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of: growing a p-type epitaxial layer above the n-type epitaxial layer, with a p-n junction between the n-type and p-type epitaxial layers. One who is skilled in the art would be motivated to form a p-n junction, a structure fundamental to the performance of many semiconductor functions, on the SiC substrate.

42. As to claims 16, Powell dose not expressly disclose growing an n-type epitaxial layer on the twice-etched surface. However, Powell's method is directed at producing atomically-flat, low-defect single crystal surfaces (column 7, lines 35-37) to produce a large variety of semiconductor devices (column 3, lines 4-17). Powell further teaches that additional growth procedures can produce multi-layered doped SiC structures (column 7, lines 54-56). Streetman further

teaches most semiconductor devices contain at least one p-n junction, which is fundamental to the performance of functions such as rectification, amplification, switching, and other functions (page 130). Streetmen further teaches that epitaxially grown junctions are widely used to form a sharp, single crystal junction by changing doping during crystal growth (page 131). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of: growing an n-type epitaxial layer on the twice-etched surface. One who is skilled in the art would be motivated to form a p-n junction, a structure fundamental to the performance of many semiconductor functions, on the SiC substrate.

43. As to claims 17 and 30, Powell does not expressly disclose growing a second conductive epilayer above the first conductive epilayer and having the opposite conductivity type from the first conductive epilayer. However, Powell's method is directed at producing atomically-flat, low-defect single crystal surfaces (column 7, lines 35-37) to produce a large variety of semiconductor devices (column 3, lines 4-17). Powell further teaches that additional growth procedures can produce multi-layered doped SiC structures (column 7, lines 54-56). Streetman further teaches most semiconductor devices contain at least one p-n junction, which is fundamental to the performance of functions such as rectification, amplification, switching, and other functions (page 130). Streetmen further teaches that epitaxially grown junctions are widely used to form a sharp, single crystal junction by changing doping during crystal growth (page 131). Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to include the step of: growing a second conductive epilayer above the first conductive epilayer and having the opposite conductivity type from the first conductive epilayer. One who is skilled in the art would be motivated to form a p-n junction, a structure fundamental to the performance of many semiconductor functions, on the SiC substrate.

Conclusion

44. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Larkin et al. (U.S. Patent No. 5,709,745) discloses a method for the chemical vapor deposition of SiC crystals. Kitou et al. (U.S. Patent No. 5,944,890) discloses a method for growing single crystal SiC. Augustine et al. (U.S. Patent No. 5,895,583) discloses a method of preparing a SiC wafer derived from a boule. Brewer (U.S. Patent Appl. Pub. No. 2003/0062335) discloses a process for smoothing a SiC substrate with plasma etching.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC

EBC
Feb. 22, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER